# Yang **HE**

Ph.D Student · University of Technology Sydney

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## Summary


I am a second-year Ph.D student at Centre for Artificial Intelligent, University of Technology Sydney (UTS), Australia, under the supervision of Prof. Yi Yang. My research interests include machine learning, deep learning and computer vision.


## Education

**UTS (University of Technology Sydney)** — *Sydney, Australia*

Ph.D in Computer Science — *Aug. 2017 - Exp. Aug. 2021*

**USTC (University of Science and Technology of China )** — *Hefei, China*

M.S. in Electronic Engineering — *Sep. 2014 - Jul. 2017*

- 2016 National Scholarship (3%), Hua Wei Scholarship (5%)

**USTC (University of Science and Technology of China )** — *Hefei, China*

B.S. in Electronic Engineering — *Sep. 2010 - Jul. 2014*

- National Scholarship for Encouragement (5%, twice)

## Research Experience

**UTS (University of Technology Sydney)** — *Sydney, Australia*

Research Assistant, Advisor: Prof. Yi Yang, Liang Zheng — *Aug. 2017 - PRESENT*

- Neural network compression and acceleration via filter pruning.

**USTC (University of Science and Technology of China)** — *Hefei, China*

Research Assistant, Advisor: Prof. Gang Wang — *Aug. 2014 - Jul. 2017*

- Designed passive identification tag for integration into aluminum blister medicine package.

**HKBU (Hong Kong Baptist University)** — *Hong Kong*

Research Intern: Advisor: Prof. Jiming Liu (IEEE Fellow) — *Jul. 2016 - Sep. 2016*

- Researched and simulated the Epidemic models including SIS, SIR etc. to understand and predict the epidemic patterns.

**USTC (University of Science and Technology of China)** — *Hefei, China*

Research Assistant, Advisor: Prof. Jian Li (IEEE Fellow) — *Oct. 2015 - Jan. 2016*

- Designed digital system to control the chip and to process the data to detect brains of patients with suspected stroke.

**USTC (University of Science and Technology of China)** — *Hefei, China*

Project Leader for the National Innovation Experiment Program — *May 2012 - Mar. 2014*

- Our team consisted of three undergraduate students and two master students.
- Designed a portable four-channel video acquisition and storage system.

**USTC (University of Science and Technology of China)** — *Hefei, China*

Undergraduate Research Program — *Jun. 2013 - Oct. 2013*

- Designed and Implemented MIPS32 CPU with Verilog, eventually handled fifteen different CPU instructions.

## Publications


[1] Yang He, Guoliang Kang, Xuanyi Dong, Yanwei Fu, and Yi Yang. Soft filter pruning for accelerating deep convolutional neural networks. In *International Joint Conference on Artificial Intelligence (IJCAI)*, pages 2234–2240, 2018.

[2] Yang He, Ping Liu, Ziwei Wang, Zhilan Hu, and Yi Yang. Filter pruning via geometric median for deep convolutional neural networks acceleration. In *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, 2019.